IN THE CLAIMS

Please amend the claims as follows:

1. A method for reducing the power consumption in a state retaining circuit during a standby mode, comprising:
in an active state, providing a regular power supply (VDD) and a standby power supply (VDD_STANDBY) to the state retaining circuit;
for a transition from an active state to a standby state, decreasing the regular power supply to ground level and maintaining the standby power supply (VDD_STANDBY) thus providing circuit elements (36, 142, 78, 85) of the state retaining circuit with enough power for retaining the state during standby mode; and
for a transition from the standby state to the active state, increasing the regular power supply (VDD) from its ground level to its active level.

2. The method of claim 1, wherein the standby power supply (VDD_STANDBY) is decreased from an active level to a lower level in moving from an active state to a standby state, the lower level being sufficient for retaining the state; and the standby power supply (VDD_STANDBY) is increased from the lower level to the active level in returning back into the active mode.

3. The method of claim 2, wherein the step of decreasing the standby power supply (VDD_STANDBY) takes place after the regular power supply (VDD) has settled at a ground level; the method further comprising the step of increasing the regular power supply (VDD) to an active level after the standby power supply (VDD_STANDBY) has settled at its active level upon returning back into the active mode.

4. The method of claim 1, wherein a control signal is held during standby mode.

5. The method of claim 4, wherein said control signal is held at a predetermined >low= level during standby mode.

6. The method of claim 4~~ or 5~~, wherein said control signal is held during standby mode by means external to said state retaining circuit.

7. The method of claim 4~~ or 5~~, wherein said control signal is held during standby mode by means (200, 201) provided within said state retaining circuit.

8. The method of clam 7, wherein said means for holding said control signal during standby mode comprises at least one transistor (200) having a gate terminal (201) connected to a standby signal, and arranged to be switched >on= during standby and switched >off= otherwise, the drain or source terminal of said transistor (200) being connected to a line having a voltage level at which said control signal is required to be held.

9. The method of claim 8, wherein said voltage level is substantially ground.

10. The method of claim 9, wherein said transistor is an n-channel MOSFET (200) having a gate terminal (201) connected to a standby signal which is >high= during standby and >low= otherwise, and a source terminal connected to ground.

11. A state retaining circuit, comprising:

a control unit (1) for providing at least one control signal;

a data input unit (3) for providing at least one input signal;

a data output unit (7) for providing at least one output signal;

a data storage unit (5) for holding at least a part of the state of the circuit during a standby mode;

first means for coupling a power supply from a regular power supply (VDD) to the circuit elements during an active mode;

second means for coupling a power supply from a standby power supply (VDD_STANDBY) to at least a part of the data storage unit (5) during the active mode and the standby mode.

12. The circuit of claim 11, wherein the control unit (1) is connected to the regular power supply (VDD) and to the standby power supply (VDD_STANDBY) for retaining a state of the control signal (CKPI/CKPNI) during the standby mode.

13. The circuit of claim 11, wherein the data input unit (3) is connected to the regular power supply (VDD).

14. The circuit of claim 11, wherein the data input unit (3) is connected to the control signal (CKPI/CKPNI).

15. The circuit of claim 11, wherein the data storage unit (5) is connected to the regular power supply (VDD) and to the standby power supply (VDD_STANDBY).

16. The circuit of claim 11 ~~or 15~~, wherein the data storage unit (5) comprises a serial circuit (78, 85) for retaining the inverted data input signal.

17. The circuit of claim 11, wherein the data output unit (7) comprises at least one input terminal for receiving a signal from the data storage unit (5), and at least one output terminal (166) for outputting the received signal from the state holding unit (5).

18. The circuit of ~~any of the claims 11 to 17~~claim 11, wherein a selection of circuit elements of the state retaining circuit have a higher threshold voltage than circuit elements not belonging to the selection.

19. The circuit of ~~any one of claims 11 to 18~~claim 11, comprising means (200) for holding said control signal at a predetermined level during standby.

20. The circuit of claim 19, wherein said means (200) for holding said control signal is included in said control unit (1).

21. The circuit of claim 19~~ and claim 20~~, wherein said means (200) for holding said control signal is connected to a standby signal which is >high= during standby mode and >low= otherwise.

22. The circuit of ~~any one of claims 11 to 21~~claim 11, including means (300, 400, 500, 600) for providing additional current to the circuit during active mode, so as to reduce the current requirement from said standby power supply.

23. An electronic device (200), comprising:

a regular power supply (220, VDD);

a standby power supply (222, VDD_STANDBY); a first circuit portion (240) coupled to the regular power supply (220, VDD); a second circuit portion (260) coupled to the regular power supply (220, VDD), the second circuit portion (260) comprising

a state retaining circuit for retaining at least a part of a state of the first circuit portion (240) during a standby mode of the electronic device (200), the state retaining circuit comprising :

a control unit (1) for providing at least one control signal;

a data input unit (3) for providing at least one input signal;

a data output unit (7) for providing at least one output signal;

a data storage unit (5) for holding at least a part of the state of the first circuit portion (240) during the standby mode;

the regular power supply (VDD, 220) being arranged to supply power to the data storage unit (5) during an active mode of the electronic device (200);

the standby power supply (VDD_STANDBY, 222) being arranged to supply power to at least a part of the data storage unit (5) during the active mode and the standby mode.

24. An electronic device as claimed in claim 23, wherein the standby power supply (VDD_STANDBY, 222) is arranged to provide a reduced power to the at least part of the state retaining circuit (5) during the standby mode.

25. An electronic device as claimed in claim 23, characterized in that a selection of circuit elements of the state retaining circuit are located in a separate well of the second circuit portion (240).